TOPIC
EMBEDDED PRODUCTS

Embedded
in your future

Dyplo® for PC/FPGA

DYnamic Process LOader

- The next step in data and signal acceleration
- Simplified FPGA design integration in PC software applications
- Out-of-the-box integration of PC & FPGA via PCI Express
- Proven significant development time reduction
- FPGA programming made software-friendly
- Runtime re-use of FPGA fabric
- GPU like programming convenience with FPGA performance superiority
- Plug-in IP blocks for zero integration effort
- Architectural exploration freedom

The Dyplo® concept

Dyplo is part of a rapidly growing ecosystem for embedded acceleration solutions by Topic Embedded Products. The Dyplo concept provides developers with the ability to connect various processing units and distribute and control processes with our Dynamic Process Loader. Dyplo enables you to get the maximum out of your platform of choice, achieving the most flexible and best possible technical solution for your application. With Dyplo you integrate in a transparent and easy to program way FPGA functions in your PC based software application. You can choose for a full C-to-FPGA design flow or an HDL implementation flow of your choice implementing core execution functions.

PC/FPGA integration via PCI EXPRESS

A standard x86 based PC in combination with an FPGA connected via PCI Express forms a powerful number crunching platform. The programming model as well as the basic infrastructure require a significant design effort to realize and asks for many different skills. Dyplo bridges this gap seamlessly, provides a user-friendly programming API on the PC software development side and a sophisticated and easy-to-use infrastructure on the FPGA. By using actively Partial Reconfiguration technology of Xilinx, operating system like functional behavior like threading and dynamic task switching is enabled.

This solution with both CPU and FPGA coupled tightly together offers many processing acceleration opportunities. FPGAs are typically used to resolve complex calculation tasks with unsurpassed performance. FPGA processing solutions have become the industries choice across many different domains. Combined with PC programming convenience a huge potential of calculation power is available at your fingertips. The only down part is the traditionally difficult programming model. But that is solved by using Dyplo for PC/FPGA.

Dyplo for PC/FPGA is based on a custom developed PCI Express controller core using a straightforward efficient DMA engine for high performance data transport between the FPGA and a host running Linux or Windows. The FPGA designer, as well as the application developer interact with the core using a well-defined and common API: The FPGA application logic connects to the IP core through standard AXI Stream interfaces; the API on the host PC performs plain stream operations. Streaming data moves naturally between the FPGA user logic and the software streams opened by the software application. The interface is user configurable using generic parameters on the HDL core instantiation. The number of streams, their direction, the data width, bandwidth expectations and other parameters can be specified here. The API can read these parameters from the core and initializes accordingly.

Visit *www.dyplo.com* for more background information and to request an evaluation license.

Windows

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Typical applications

- Data acquisition
- HPC (High Performance Computing)
- FPGA control from host, easy design of peripherals
- Interface with dedicated hardware
- Logic verification on hardware (Hardware-in-the-Loop)

Benefits

Dyplo enables you to postpone architectural choices to a later stage as you can move functionality across the platform when performance issues arise or are identified.

AXI compliant

Adding IP blocks to your Dyplo infrastructure is simple. As long as the code is AXI compliant, hassle free integration is guaranteed.

Data acceleration

The amount of data increases day by day. The internal structures of the FPGAs are extremely suitable for data processing in terms of available processing power, low energy consumption and memory bandwidth. Downsides: programming FPGAs is complex, and they have typically fixed functionality. Dyplo gives the FPGA this flexibility, totally controlled and managed. The next step in data acceleration is enabled by Dyplo giving the FPGA the flexibility to process large data sets with low energy consumption.

Partial Reconfiguration

Partial reconfiguration means that you can re-use, start, stop or copy parts of the cores of your FPGA dynamically when required. For many years, utilization of this specific area of FPGAs has been out of reach for many FPGA users. Dyplo gives you an easy way to benefit from partial reconfiguration. From a user perspective, simply earmarking blocks for acceleration allows the Dyplo system to accelerate your application as and when it is required. *Imagine, reducing the size of your fabric with 60% while only using 40% of your fabric simultaneously!*

OS Independency

The PC/FPGA version of Dyplo is managed by Linux or Windows. Dyplo is and will be available for many operating systems. If our roadmap does not meet your timeline, it will take only a couple of weeks work for us.

From a system perspective

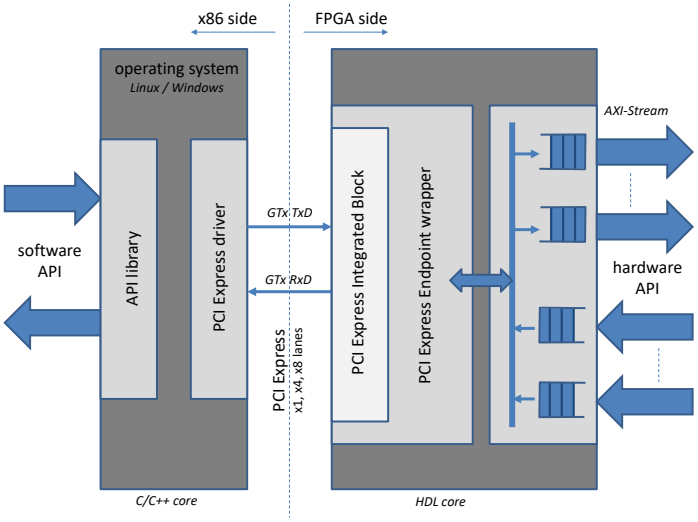
Suspend architectural choices to a much later stage as you can move functionality across platform when bottle-necks arise.

From a hardware perspective

Your field of expertise will be valued more, and used more frequently by enabling software engineers to access parts of your domain in a controlled and managed manner. You can focus on your expertise, while full integration of your state of the art work is enabled by the Dyplo Framework.

From a software perspective

Programming an FPGA is totally different compared to a PC. Dyplo extends the FPGA domain to your software domain. The infrastructure is ready to use, and the processor blocks are designed and can be managed in such a way as if you were using software processors, but then much, much more powerful. Typically, FPGA's have a fixed behavior once programmed. Dyplo offers an ease way to reprogram parts of your FPGA resources, runtime if you like!



Part of the ecosystem

Dyplo is a product of Topic Embedded Products. The eco-system of Software Solutions, System on Modules, Carrier Boards, development Kits and IP blocks are all compatible and combinable. We take the greatest care in making sure both the hardware and the software part of our solutions you buy is of high quality and includes the latest updates available. Our online store and wordwide distribution network help you even further to accelerate your development, with simple access to all our products. If you need any assistance developing your system, our Dsign department can support you by developing parts of your system as a service.

Visit www.topic.nl for more information on our ecosystem and how this can be beneficial for you.